Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended) An integrated circuit for a digital still camera, comprising:

(a) a first programmable processor programmed to run control functions, said first processor coupled to a user interface, a controller for memory, and a controller for image acquisition; ~~and~~

(b) a second programmable processor programmed to run image processing and compression functions, said second processor coupled to said first processor; and

(c) a third processor coupled to said second processor, said third processor including at least four parallel multiply and accumulate units.

Claim 2 (cancelled)

Claim 3 (currently amended) An integrated circuit for a digital still camera, ~~The integrated circuit of claim 1,~~ comprising:

(a) a first programmable processor programmed to run control functions, said first processor coupled to a user interface, a controller for memory, and a controller for image acquisition;

(b) a second programmable processor programmed to run image processing and compression functions, said second processor coupled to said first processor; and

(c) an image compression unit separate from said second processor, said compression unit arranged to compress acquired images for storage in a memory and to decompress said compressed acquired images in said memory for restorage in said memory.

Claim 4 (currently amended) An integrated circuit for a digital still camera, ~~The integrated circuit of claim 1, further~~ comprising:

(a) a first programmable processor programmed to run control functions, said first processor coupled to a user interface, a controller for memory, and a controller for image acquisition;

(b) a second programmable processor programmed to run image processing and compression functions, said second processor coupled to said first processor; and

(c) a digital image processing unit separate from said first and second processors, said image processing unit arranged for real-time image sequence (video) processing, said image processing unit controlled in real-time by said first processor

Claim 5 (original) The integrated circuit of claim 1, further comprising:

(a) an audio input coupled to said second processor, said second processor programmed to decode audio and said first processor programmed to output said decoded audio.

Claim 6 (original) The integrated circuit of claim 1, further comprising:

(a) camera peripherals including IfSA, USB, NTSC/PAL encoder, and compact flash/smart media interface.